

FIG. 1

FIG. 2 is a block diagram of a system for error correction. The system includes a CODEWORD DATA input, a STAGE 12 block, a STAGE 30 block, a PROCESSOR 40 block, and an ERROR CORRECTION PROCESSOR block. The CODEWORD DATA input is connected to STAGE 12. STAGE 12 outputs $r_2(x)$, $q_1(x)$, $r_1(x)$, and $r_2(x)*g_1(x)$ to the PROCESSOR 40. STAGE 30 outputs $q_1(x)$ to the PROCESSOR 40. The PROCESSOR 40 outputs ECC to the ERROR CORRECTION PROCESSOR. The ERROR CORRECTION PROCESSOR outputs ERROR-FREE DATA.

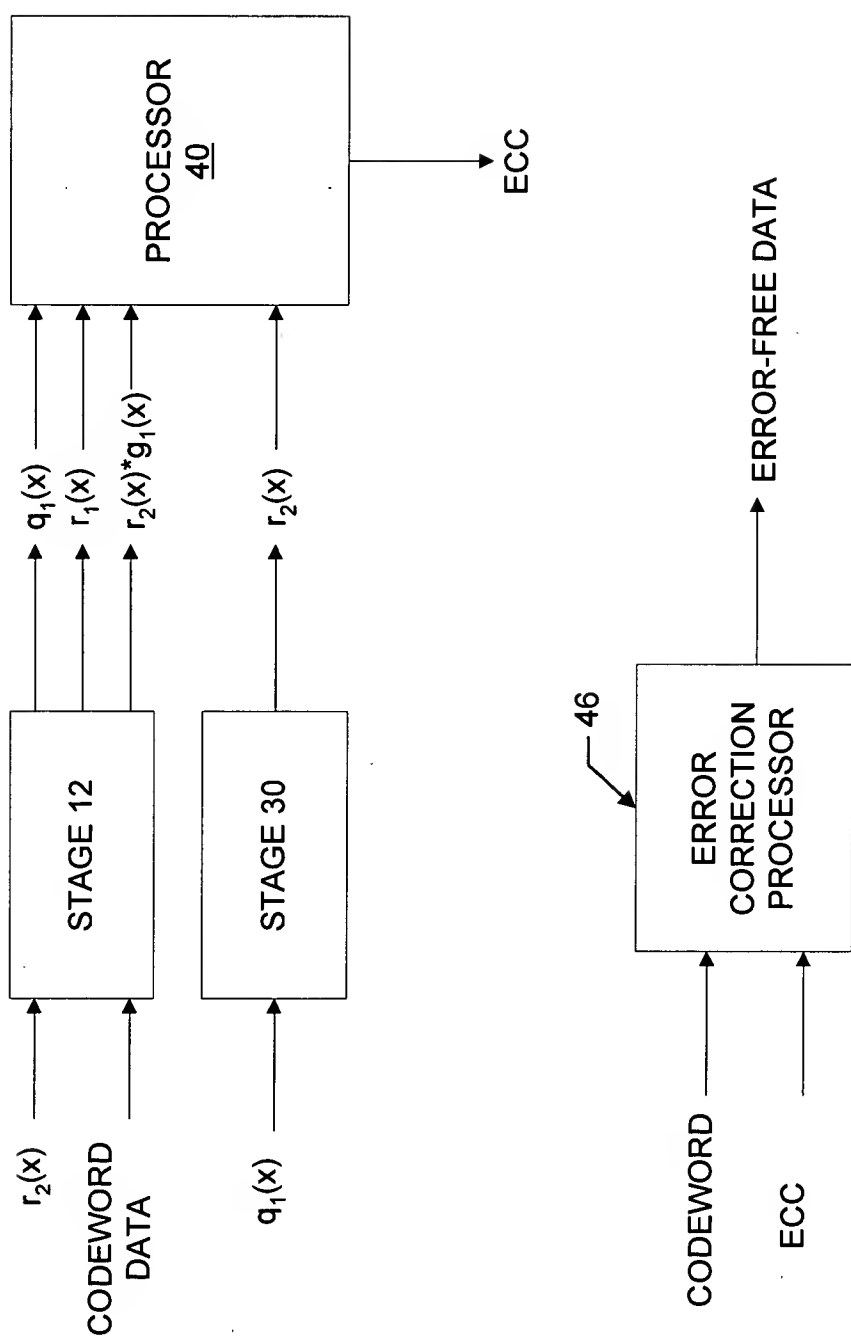


FIG. 2

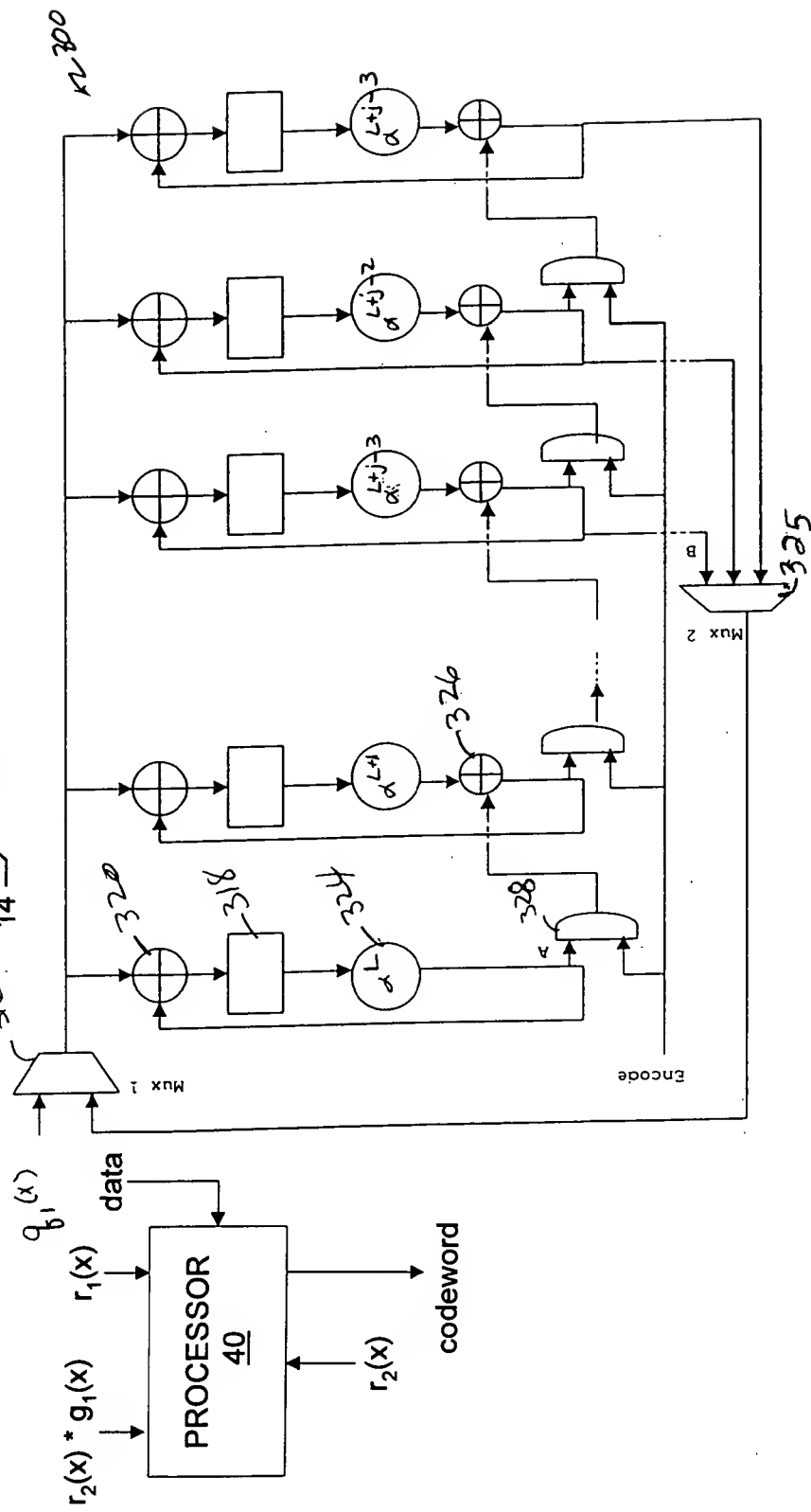
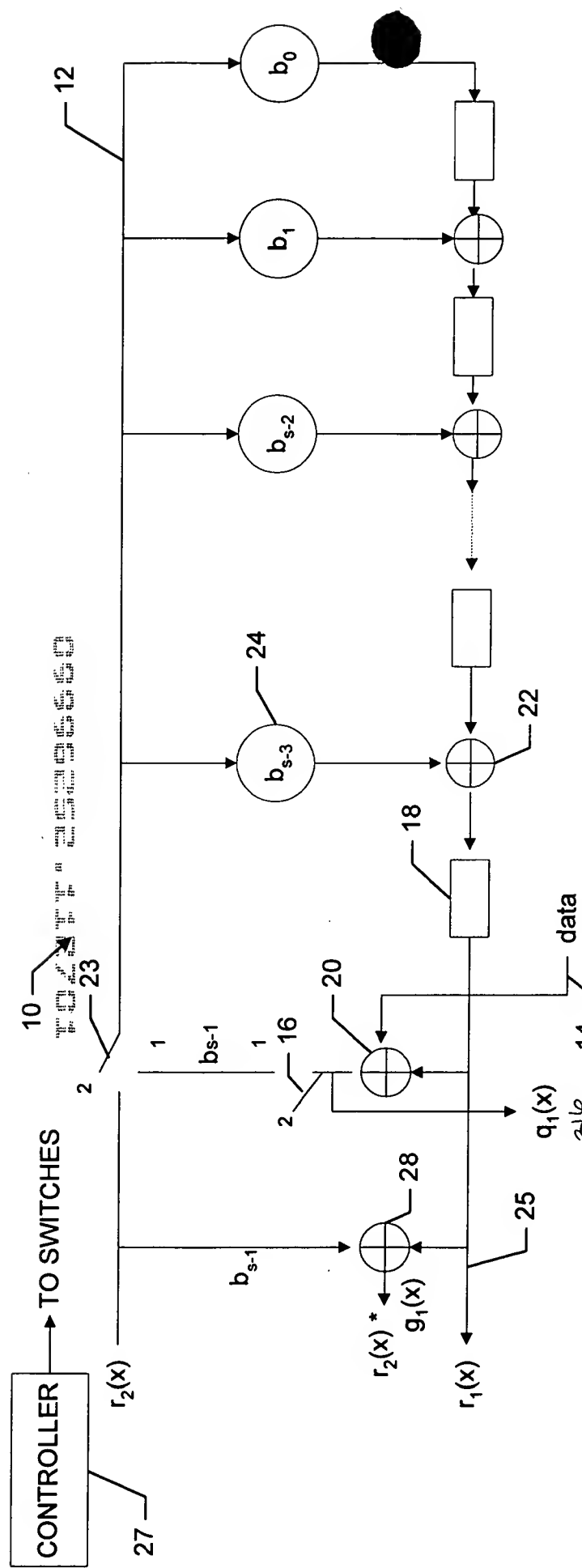


FIG. 3

FIG. 4 is a block diagram of a system for error correction.

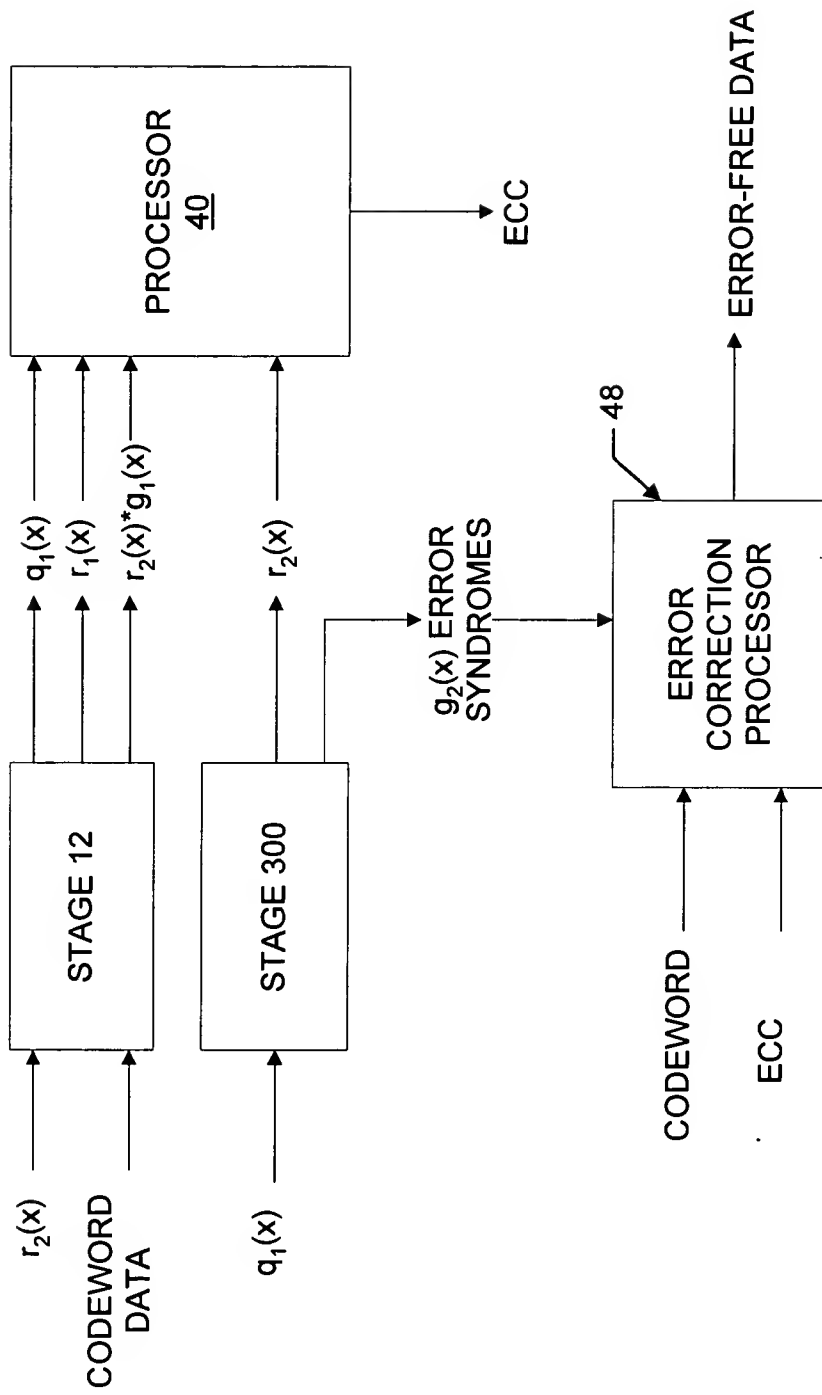


FIG. 4